CLAIMS

What is claimed is:

1. A method of reducing power consumption in an integrated circuit communication link having a logic circuitry, the logic circuitry including supply-voltage-critical logic circuitry and non-supply-voltage-critical logic circuitry, the method comprising the steps of:

synthesizing the integrated circuit to identify the supply-voltage-critical logic circuitry;

isolating the supply-voltage-critical logic circuitry from the non-supply-voltage-critical logic circuitry, the supply-voltage-critical logic circuitry being driven by a first supply voltage and the non-supply-voltage-critical logic circuitry being driven by a second supply voltage, the first supply voltage being greater than the second supply voltage;

embedding a voltage regulator in the communication link for supplying the second voltage; and

selectively interfacing the supply-voltage-critical logic circuitry with the non-supply-voltage-critical logic circuitry using level shifters.

2. The method of Claim 1 wherein the first voltage is supplied to the communication link.

3. The method of Claim 2 wherein the first voltage is used to generate the second voltage.

4. The method of Claim 3 wherein the selectively interfacing step includes the step of selecting a minimal number of points at which the supply-voltage-critical logic circuitry interfaces with the non-supply-voltage-critical logic circuitry.

5. The method of Claim 4 wherein a level shifter is used at each interfacing point.

6. The method of Claim 5 wherein the communication link is on a chip, the chip having a multiplicity of communication links, a plurality of the multiplicity of the communication links sharing the embedded voltage regulator.

7. An integrated circuit communication link comprising:

a first logic circuit group characterized by supply voltage critical circuitry and being driven by a first voltage;

a second logic circuit group being driven by a second voltage, the first voltage being higher than the second voltage;

an embedded voltage regulator for supplying the second voltage; and

at least one level shifter for interfacing the first logic circuit group with the second logic circuit group.

8. The communication link of Claim 7 wherein the first voltage is supplied to the communication link.

9. The communication link of Claim 8 wherein the first voltage is used to generate the second voltage.

10. The communication link of Claim 10 wherein the first logic circuit group interfaces with the second logic circuit group at a plurality of points, the plurality of points being a minimal number of points.

11. The communication link of Claim 10 wherein a level shifter is used at each interfacing point.

12. The communication link of Claim 12 wherein the communication link is on a chip, the chip having a multiplicity of communication links, a plurality of the multiplicity of the communication links sharing the embedded voltage regulator.

13. A chip comprising:

a plurality of embedded communication links, the links including each:

a first logic circuit group characterized by a supply voltage critical circuitry and being driven by a first voltage;

a second logic circuit group being driven by a second voltage, the first voltage being higher than the second voltage;

an embedded voltage regulator for supplying the second voltage; and

at least one level shifter for selectively interfacing the first logic circuit group with the second logic circuit group.

14. The chip of Claim 13 wherein the first voltage is supplied to the communication link.

15. The chip of Claim 14 wherein the first logic circuit group interfaces with the second logic circuit group at a plurality of points, the plurality of points being a minimal number of points.

16. The chip of Claim 15 wherein a level shifter is used at each interfacing point.

17. The chip of Claim 16 wherein a plurality of the communication links share the embedded voltage regulator.

18. A method of reducing power consumption in an integrated circuit communication link having logic circuitry, the logic circuitry including supply-voltage-critical logic circuitry and non-supply-voltage-critical logic circuitry, the method comprising the steps of:

determining and isolating the supply-voltage-critical logic circuitry from the non-supply-voltage-critical logic circuitry, the supply-voltage-critical logic circuitry being driven by a first supply voltage and the non-supply-voltage-critical logic circuitry being driven by a second supply voltage, the first supply voltage being greater than the second supply voltage;

embedding a voltage regulator in the communication link for supplying the second voltage: and

selectively interfacing the supply-voltage-critical logic circuitry with the non-supply-voltage-critical logic circuitry using level shifters.

19. The method of Claim 18 wherein the determining step includes the step of synthesizing the communication link using the second voltage to identify the supply-voltage-critical logic circuitry.

20. The method of Claim 19 wherein the communication link is on a chip, the chip having a multiplicity of communication links, a plurality of the multiplicity of the communication links sharing the embedded voltage regulator.